In the Claims:

Please cancel claims 1-11. Please amend claims 12, 14, and 18-19. Please add new claims 21-31. The claims are as follows.

1-11. (Canceled)

12. (Currently amended) A method of reduced pin count testing ~~the~~ a chip-to-package connectivity of a semiconductor device, the method comprising:

providing an I/O driver and an I/O receiver on the semiconductor device, wherein a common I/O of the semiconductor device is electrically coupled to the driver and to the receiver, and wherein the common I/O is electrically interposed between the driver and the receiver;

launching a transition signal from ~~a common I/O~~ the driver ~~on the packaged semiconductor device~~;

observing a response of the transition signal at a point within the semiconductor device; and

determining whether a chip-to-package connection associated with the common I/O is faulty from the response of the transition signal.

13. (Previously presented) The method of claim 12, further comprising driving the transition signal with a weak driver.

14. (Currently amended) An apparatus configured to launch a test signal to a common I/O of a semiconductor device from [[a]] an I/O driver on the semiconductor device which is associated with the common I/O using reduced pin count testing, the apparatus comprising:

a test fixture configured to couple to [[a]] the common I/O of the semiconductor device;

an I/O receiver on the semiconductor device, wherein the common I/O is electrically coupled to the driver and to the receiver, and wherein the common I/O is electrically interposed between the driver and the receiver;

a weak driver impedance coupled between the driver and the test fixture;

wherein the apparatus is configured to launch the test signal through the weak driver impedance and the common I/O to the test fixture and evaluate a characteristic of a response to the test signal to determine whether a chip-to-package connection associated with the common I/O is faulty.

15. (Previously presented) The apparatus of claim 14, wherein the weak driver impedance includes a switchable impedance.

16. (Original) The apparatus of claim 14, wherein the weak driver impedance is an impedance having a resistive value of 1 KΩ or more.

17. (Original) The apparatus of claim 16, wherein the weak driver impedance is approximately 10 KΩ or more.

18. (Currently amended) The apparatus of claim 14, further comprising a fixture impedance coupled between the test fixture and ~~at least one of~~ the semiconductor device ~~and a potential relative to the semiconductor device~~.

19. (Currently amended) The apparatus of claim 18, wherein the fixture impedance comprises a capacitor ~~coupled between the common I/O and a fixed potential relative to the semiconductor device~~.

20. (Previously presented) The apparatus of claim 14, wherein the weak driver impedance includes a variable impedance.

21. (New) The apparatus of claim 14, wherein the weak driver impedance is on the semiconductor device.

22. (New) The apparatus of claim 14, wherein the weak driver impedance is electrically interposed between the driver and the common I/O.

23. (New) The apparatus of claim 14, further comprising a point at which test signal is adapted to be measured, wherein the point is electrically interposed between the weak driver impedance and the common I/O.

24. (New) The apparatus of claim 14, further comprising an observation latch on the semiconductor device, wherein the observation latch is adapted to be triggered when the test signal reaches a predetermined threshold.

25. (New) The method of claim 12, further comprising:

providing an observation latch on the semiconductor device; and

triggering the observation latch when the transition signal reaches a predetermined threshold.

26. (New) The method of claim 12, providing a weak driver impedance on the semiconductor device.

27. (New) The method of claim 26, wherein the weak driver impedance is electrically interposed between the driver and the common I/O.

28. (New) The method of claim 26, wherein the point is electrically interposed between the weak driver impedance and the common I/O.

29. (New) The method of claim 26, wherein the weak driver impedance is an impedance having a resistive value of 1 KΩ or more.

30. (New) The method of claim 26, further comprising providing a fixture impedance coupled between a test fixture and the semiconductor device, wherein said launching comprises launching the transition signal from the driver through the weak driver impedance and the common I/O to the test fixture.

31. (New) The method of claim 30, wherein the fixture impedance comprises a capacitor.